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To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

Fr: George O. Saile, Reg. No. 19,572
20 McIntosh Drive
Poughkeepsie, N.Y. 12603

Subject: Serial No. 09/938,040 08/23/01

Mark Hatzilambrou, Chester Leung,
Rajan Walia, Wee Liang Lien,
Subhash Rustogi, M. Radhakirishnan

ESD PROTECTION SYSTEM FOR HIGH
FREQUENCY APPLICATIONS

Grp. Art Unit: 2836

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

The following four U.S. Patents use a single main shunt between two power supply nodes and couple other power supplies (including the Vdd supplies) via diodes or bridge circuits:

1) U.S. Patent 5,740,000 to Stackhouse et al., "ESD Protection System for an Integrated Circuit with Multiple Power Supply Networks."

2) U.S. Patent 5,654,862 to Worley et al., "Method and Apparatus for Coupling Multiple Independent On-Chip Vdd Busses to an ESD Core Clamp."
3) U.S. Patent 5,530,612 to Maloney, "Electrostatic Discharge Protection Circuits Using Biased and Terminated PNP Transistor Chains."
4) U.S. Patent 5,515,225 to Gens et al., "Integrated Circuit Protected Against Electrostatic Overvoltages."

The following two U.S. Patents disclose power shunt circuits:

1) U.S. Patent 5,946,177 to Miller et al., "Circuit for Electrostatic Discharge Protection."
2) U.S. Patent 5,508,649 to Shay, "Voltage Level Triggered ESD Protection Circuit."

U.S. Patent 5,744,842 to Ker, "Area-Efficient VDD-to-VSS ESD Protection Circuit," discusses an electrostatic discharge (ESD) protection circuit which forms part of an integrated circuit having a VDD line and a VSS line.

U.S. Patent 5,559,659 to Strauss, "Enhanced RC Coupled Electrostatic Discharge Protection," discloses an integrated circuit ESD protection technique including a protection circuit having a series resistor-capacitor circuit connected between power supply bondpads.

U.S. Patent 6,091,593 to Lin, "Early Trigger of ESD Protection Device by a Negative Voltage Pump Circuit," discloses an RC timed ring-oscillator charge pump for inducing turn-on in MOS or bipolar protection devices.

U.S. Patent 6,072,682 to Ravanelli et al., "Protection Circuit for an Electric Supply Line in a Semiconductor Integrated Device," describes an all NMOS RC-triggered source-follower shunt.

U.S. Patent 6,014,298 to Yu, "Electrostatic Protection Circuit of an Integrated Circuit," discloses an RC timed switch to be placed in series between power Vcc and circuit to be protected. The switch turns off when an ESD is detected to prevent discharge going through the core circuit.

U.S. Patent 5,986,861 to Pontarollo, "Clamp," presents a simple clamp, with a PMOS final transistor and NMOS inverter triggered by RC.

U.S. Patent 5,907,464 to Maloney et al., "MOSFET-Based Power Supply Clamps for Electrostatic Discharge Protection of Integrated Circuits," describes a shunt circuit with a PMOS final driver and timed by a PMOS resistor/generic capacitor time constant.

U.S. Patent 5,745,323 to English et al., "Electrostatic Discharge Protection Circuit for Protecting CMOS Transistors on Integrated Circuit Processes," teaches an input line protection circuit which uses RC-timed PMOS and NMOS transistors to discharge ESD current to the Vdd and Vss power rails.

U.S. Patent 5,287,241 to Puar, "Shunt Circuit for Electrostatic Discharge Protection," discloses a PMOS final driver triggered and timed by a PMOS resistor/NMOS capacitor RC.

U.S. Patent 5,255,146 to Miller, "Electrostatic Discharge Detection and Clamp Control Circuit," describes an NMOS final driver with three RC timers, feedback loop, and NAND gate triggering to detect the rise time of the ESD, to insure that the ESD is longer than a typical noise pulse.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761